



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/815,871

04/02/2004

Koji Ozaki

251088US6

1011

22850

7590

04/18/2006

OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER

SCHLIE, PAUL W

ART UNIT

PAPER NUMBER

2186

DATE MAILED: 04/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/815,871	Applicant(s) OZAKI, KOJI	
	Examiner Paul W. Schlie	Art Unit 2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 4/02/04.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-22 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 02 April 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>1</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-22 have been examined.

Priority

2. Applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d) is acknowledged.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukunaga et al. (4,481,573).

As per independent claims 1, 14, 16, 18, 20-22, Fukunaga et al. teaches a system and/or methods comprising a processor utilizing a Harvard Architecture supporting distinct logical/physical instruction and data memory interfaces (as are inherently characteristic of such an architecture) each correspondingly interconnected to an independent cache utilizing virtual addresses as the basis upon which previously addressed values are cached, where upon a cache miss said virtually addressed value will be first accessed from a commonly physically addressed address space utilizing a Translation Look-aside Buffer (TLB), and that such a translation may be performed utilizing either a common TLB (where one of ordinary skill in the art understands that physically distinct addresses may be orthogonally cached by tagging its cached representation), or physically distinct TLBs associated with each cached interface

Art Unit: 2186

(thereby more clearly teaching logically/physically distinct yet arithmetically equivalent virtual addresses may be independently translated to a unified physical address space, thereby a common virtual instruction and data address may be mapped to distinct physical addresses thereby logically mutually overlap, regardless of whether lesser significant bits are transposed, as such a transposition is logically transparent); where although Fukunaga et al. does not explicitly teach that such a system may be comprised within an imaging apparatus, it is considered obvious to one of ordinary skill in the art that such a processing system and/or methods as taught by Fukunaga et al. relevant to the claims may be utilized within an image processing apparatus to improve the efficiency of its processing. (See abstract, column 2 lines 56-68, and figure 1.)

As per claims 2-13 dependent on claim 1 or corresponding dependent claim inclusively, it is considered inherent that within such a system any direct and/or instruction relative virtual data address being accessed through said data interface may be distinctly or commonly orthogonally mapped to a logically mutually overlapping physical address space (as reviewed above) and that said physical address space may obviously be mapped to memory and/or I/O interfaces such that said addresses may be designated as being able to be optionally exclusively read and/or written and/or correspondingly so designated within their respectively cached lines partitioned and/or tagged in any conventionally understood manner; and further as also reviewed above, as the logical transposition of physical address bits is effectively logically transparent, such a transposition at any logical boundary is considered an obvious design choice

Art Unit: 2186

available to those of ordinary skill in the art, and thereby not considered a patentably distinguishable limitation. (Further see column 1 lines 46-49 and figures 9-17.)

As per claims 15, 17 and 19, being dependent on 14, 16, 18, or corresponding dependent claim inclusively, are considered encompassed by claims (2-13) above, these claims are rejected based upon the same arguments as correspondingly presented above.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul W. Schlie whose telephone number is 571-272-6765. The examiner can normally be reached on Mon-Thu 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 517-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


PIERRE BATAILLE
PRIMARY EXAMINER
4/15/06